DESCRIPTION

The SMCDFN10-0524P is ultra low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from over voltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients). The SMCDFN10-0524P have a typical capacitance of only 0.30pF between I/O pins. This allows it to be used on circuits operating in excess of 3GHz without signal attenuation. They may be used to meet the ESD immunity requirements of IEC 61000- 4-2, Level 4 (±15kV air, ±8kV contact discharge). The SMCDFN10-0524P will protect four lines. The SMCDFN10-0524P is in a 10-pin, RoHS/WEEE compliant, DFNWB2.5×1-10L package. It measures 2.5 x 1.0 with a nominal height of 0.50mm. The leads are spaced at a pitch of 0.5mm and are finished with lead-free pure Sn. They are designed for easy PCB layout by allowing the traces to run straight through the device. The combination of small size, low capacitance, and high level of ESD protection makes them a flexible solution for applications such as HDMI, DisplayPort ™, MDDI, and eSATA interfaces.

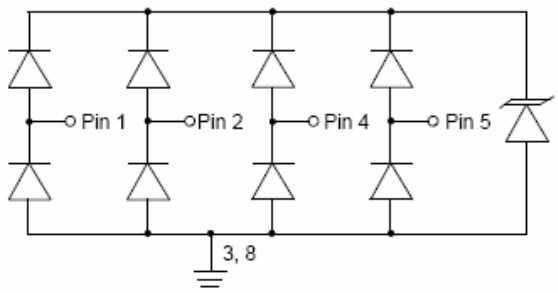
FEATURES

- **ESD protection for high-speed data lines to**
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-5 (Lightning) 5A (8/20μs)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
- **Package design optimized for high speed lines**
- **Flow-Through design**
- **Protects four I/O lines**
- **Low capacitance: 0.3pF typical (I/O to I/O)**
- **Low clamping voltage**
- **Low operating voltage: 5V**
- **Solid-state silicon-avalanche technology**

MECHANICAL CHARACTERISTICS

- **DFNWB2.5×1-10L 10-pin package**
- **RoHS/WEEE Compliant**
- **Lead Pitch: 0.5mm**
- **Lead finish: Pure Sn**
- **Marking: Marking Code**
- **Packaging: Tape and Reel**

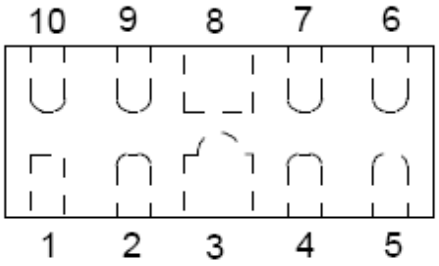
CIRCUIT DIAGRAM



APPLICATIONS

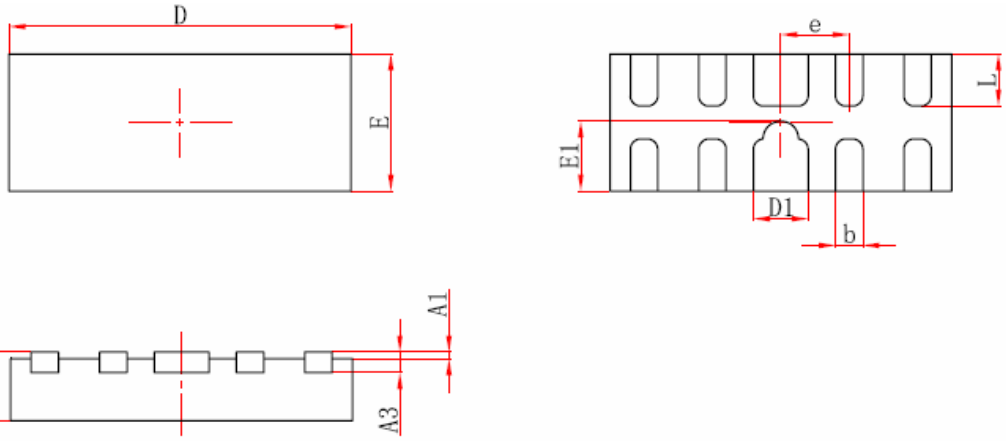
- **High Definition Multi-Media Interface (HDMI)**
- **Digital Visual Interface (DVI)**
- **DisplayPort ™ Interface**
- **MDDI Ports**
- **PCI Express**
- **eSATA Interfaces**

PIN CONFIGURATION



Pin	Identification
1, 2, 4, 5	Input Lines
6, 7, 9, 10	Output Lines (No Internal Connection)
3, 8	Ground

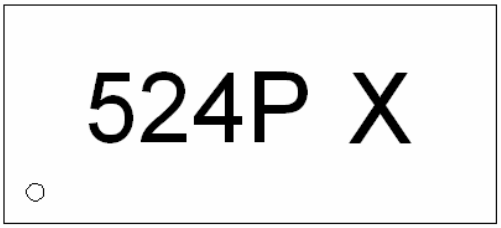
PACKAGE OUTLINES & DEMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.450	0.550	0.018	0.022
A1	0.000	0.050	0.000	0.002
A3	0.150REF.		0.006REF.	
D	2.424	2.576	0.095	0.101
E	0.924	1.076	0.036	0.042
D1	0.300	0.500	0.012	0.020
E1	0.410	0.610	0.016	0.024
k	—	—	—	—
b	0.150	0.250	0.006	0.010
e	0.500TYP.		0.020TYP.	
L	0.304	0.456	0.012	0.018

DFNWB2.5×1-10L

MARKING DIAGRAM



Where 524P is SMCDFN10-0524P

524P = Part Name
X = Date Code

Cautions: Molding resin
Epoxy resin UL:94V-0

Ordering Information:

Device	Package	Shipping
SMCDFN10-0524P	DFNWB2.5×1-10L (Pb-Free)	3000pcs / reel

For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification.

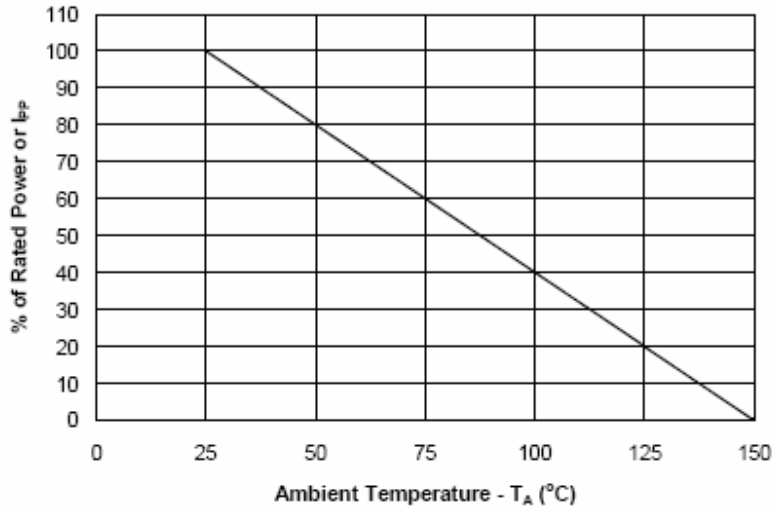
Maximum Ratings @T_A=25°C unless otherwise specified

Parameter	Symbol	Value	Unit
Peak Pulse Power (tp=8/20μs)	P_{PP}	150	W
Peak Pulse Current (tp=8/20μs)	I_{PP}	5	A
Operating Junction Temperature Range	T_J	-55 to + 150	°C
Storage Temperature Range	T_{STG}	-55 to + 150	°C

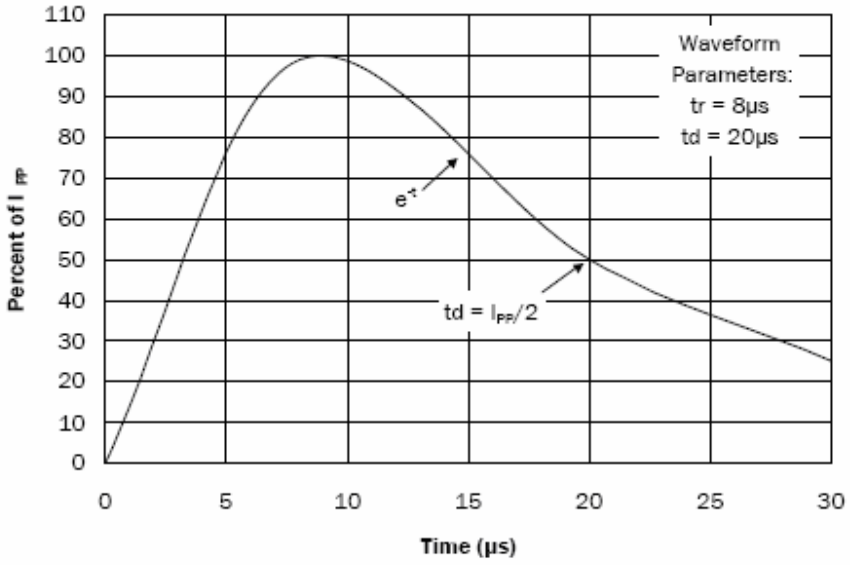
Electrical Characteristics:

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	Any I/O pin to ground	-	-	5	V
Reverse Breakdown Voltage	V_{BR}	@ I_t=1mA Any I/O pin to ground	6	-	-	V
Forward Voltage Drop	V_F	@ I_F=1mA, T = 25 ℃	-	-	0.9	V
Reverse Leakage Current	I_R	@V_{RWM} = 5V, T = 25 ℃ Any I/O pin to ground	-	-	1	μA
Clamping Voltage	V_C	@I_{PP} = 1A, tp=8/20μs Any I/O pin to ground	-	-	15	V
Junction Capacitance	C_j	@V_R = 0V, f_{SIG} = 1MHz Between I/O pins	-	0.3	0.4	pF
Junction Capacitance	C_j	@V_R = 0V, f_{SIG} = 1MHz Any I/O pin to ground	-	-	0.8	pF

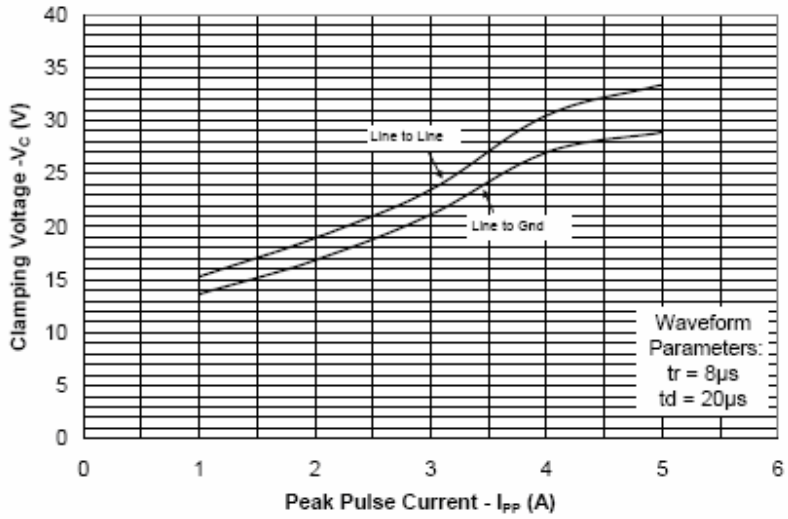
Power Derating Curve

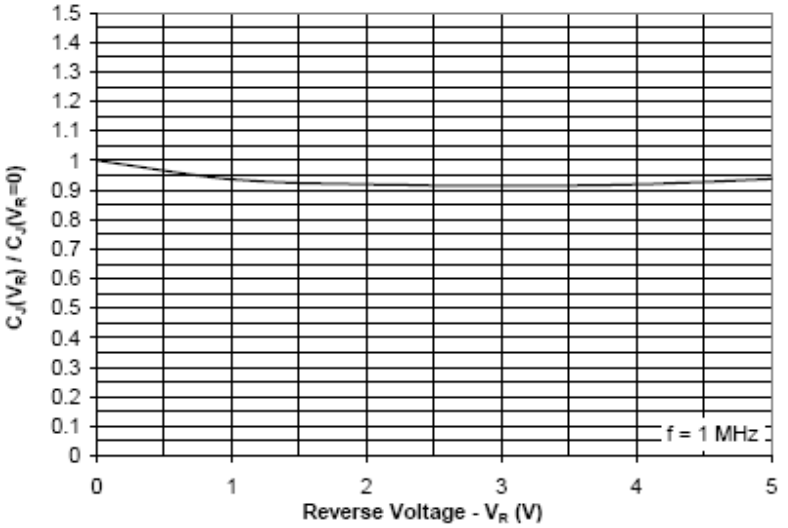


Pulse Waveform



Clamping Voltage vs. Peak Pulse Current





Technical Data ***Green Products***

Data Sheet N1513, Rev. C